METHOD FOR MEMORY ARRAY READ

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FIELD OF THE INVENTION

[001] The present invention relates generally to memory arrays and particularly to a method of reading information with neighbor effect cancellation in such memory arrays.

BACKGROUND OF THE INVENTION

[002] Memory devices, such as random access memory (RAM), read-only memory (ROM), non-volatile memory (NVM) and like, are known in the art. These devices typically provide an indication of the data stored therein by providing a readout electrical signal. A sense amplifier may be used for detecting the signal and determining the logical content of the memory cell being read.

[003] In general, sense amplifiers determine the logical value stored in a cell by comparing the output signal of the cell with a reference level. If the output signal is above the reference level, the cell is determined to be in one state, e.g., erased, and if the output is below the reference level, the cell is determined to be in another state, e.g., programmed. The reference level is typically set as a voltage or current level between the expected erased and programmed output signal voltage or current levels, and is sufficiently far from both output signal levels, so that noise on the output signal of the memory cell being read will not produce false results. As an example, the

expected memory cell output signal for its erased and programmed states may be 150mV and 50mV, respectively, and the reference level may be 100mV. In this example, if different sources of noise sources sum up and generate a noise signal of about 50mV or more then the cell may be erroneously read. To overcome such case, the noise signal generators should be suppressed or the margin between the erased and programmed state signals should be increased.

[004] In a virtual ground (VG) array, the readout of a cell may depend on the state of its neighbor cells. Therefore, a change in the state of the neighbors of a cell may affect the cell readout reliability. This undesired effect is known in the art as the "neighbor effect" (NE). The NE will be better understood by reference to Fig. 1 which is a block diagram of NVM cells in a virtual ground (VG) array. Cell MC_3 in Fig. 1 is verified to be in a specific state, e.g., programmed or erased. When MC_3 is read, the signal developed at the reading node, for example, either in the drain side or in the source side of the cell, has two components: the current of the cell itself, and the current flowing to or from neighbor cells, depending if cell MC_3 is read from the source or from the drain. Neighbor cells may share the same word line of the cell being read and may be connected, either directly or through other cells, to the reading node. For example, in the configuration of Fig. 1, cells MC_2 and MC_4 are adjacent to cell MC_3. When one or more of the neighbor cells changes from an erased state to a programmed state or vice versa, the read-out current from MC_3 may exhibit a different signal at the reading node, because the current component of its neighbor cells has changed.

[005] Thus, for example, if cell MC_3 is read out from its drain side (shown in Fig.1) then after the state of MC_2 is changed from an erased state to a programmed state, its current "contribution" to the read-out current of MC_3 may change, and therefore, the read-out for MC_3 may exhibit a different signal at the reading node. A similar effect may happen, for example, after the state of MC_4 is likewise changed for the case of source-side read. If farther cells along the same word line change their state (e.g. MC_1, MC_5, MC_6, etc., not shown in Fig. 1) they may also affect the readout of MC_3. The influence on MC_3 of such changes in the states of cells MC_1, MC_2, MC_4, MC_5 and MC_6 may not necessarily be of equal magnitude and may depend on the readout scheme, i.e. drain-side read or source-side read.

[006] A memory cell, such as MC_3 in Fig. 1, may be read from its drain side or its source side, i.e. the cell current or voltage signal may be sensed or derived from either its drain or source terminals. The NE may reduce the margin of a memory cell causing it to be read incorrectly in either of drain-side or source-side readout schemes.

[007] Several ways to reduce the NE have previously been proposed. One such suggestion to reduce the NE is, for example, to insert a voltage level that nearly equalizes the drain and source voltage of one or more of the neighbor cells. Such method is described in U.S. patents 6,351,415 and 6,510,082. However, since the reading node being sensed is transient, and therefore, its slope and level depend on data, process, and temperature factors, the drain-source voltage of the neighbor cells is typically non-zero, and some neighbor current usually exists, resulting in only partial NE reduction.

[008] Accordingly, there is a need for an efficient and reliable method for reading cells in a memory array.

SUMMARY OF THE INVENTION

[009] There is provided in accordance with embodiments of the present invention a method of reading data in a virtual ground array of memory cells comprising sensing substantially simultaneously a state of adjacent memory cells, wherein the data stored in each cell of the adjacent memory cells is in an identical state or wherein a bit stored in each cell of the adjacent memory cells is in an identical state.

[0010] There is further provided in accordance with embodiments of the present invention a method wherein sensing substantially simultaneously the state of the adjacent memory cells comprises coupling a sense amplifier to a first source/drain terminal of each cell of the adjacent memory cells, setting a voltage at a second drain/source terminal of each cell of the adjacent cells to a read level, and sensing in a reading direction the state of the adjacent cells.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features and advantages thereof, may best be understood by reference to the following non-limiting detailed description when read with the accompanied drawings in which:

[0012] Fig. 1 is a simplified block diagram demonstrating the neighbor effect (NE) in non-volatile memory (NVM) cells in a virtual ground (VG) array;

[0013] Figs. 2A and 2B are simplified block diagrams of possible methods for read operation of memory cells in a VG NVM array in a two cell per bit configuration in accordance with an embodiment of the invention, where Fig. 2A is a simplified block diagram of a source-side read operation and Fig. 2B is a simplified block diagram of a drain-side read operation;

[0014] Figs. 3A and 3B are block diagram illustrations of possible methods for read operation of memory cells in a VG NVM array in a two cell per two bits configuration in accordance with an embodiment of the invention, where Fig. 3A is a simplified block diagram of a source-side read operation and Fig. 3B is a simplified block diagram of a drain-side read operation;

[0015] Figs. 4A, 4B and 4C are block diagram illustrations of possible methods for read operation of memory cells in a VG NVM array in an N pairs of cells per one bit or per two bits configuration in accordance with an embodiment of the invention, where the cells in Fig. 4A are divided to N pairs that share the same word line, the cells in Fig. 4B are divided to N pairs that

share the same bit line, and the cells in Fig. 4C are divided to N pairs that share a combination of word lines and bit lines;

[0016] Fig. 5 is a block diagram illustration of a VG NVM array, operable in accordance with embodiments of the present invention; and

[0017] Fig. 6 is a block diagram illustration of a different configuration of a VG NVM array, operable in accordance with this embodiment of the present invention.

[0018] It will be appreciated that for simplicity and clarity of these non-limiting illustrations, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0019] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods and procedures have not been described in details so as not to obscure the present invention.

[0020] Reference is now made to Figs. 2A and 2B which are block diagram illustrations of a group of memory cells in a VG NVM array 10 being read using possible methods for read operation in a two cell (i.e., one pair) per bit configuration in accordance with an embodiment of the invention. A suitable exemplary structure of an array that may be used in accordance with this invention is such as described in U.S. Patents No. 5,963,465 or 6,633,496 which are incorporated by reference in their entireties, both of which are assigned to the same assignee as the present invention. The exemplary array may include a first plurality of word lines (WL), a second plurality of global bit lines (GBL) which may be metal, a third plurality of local bit lines (LBL) which may be formed by diffusion and a fourth plurality of select transistors.

[0021] In accordance with an embodiment of the present invention, memory cells MC_1 through MC_8 depicted in Figs. 2A and 2B may be NROM cells. NROM cells are described in various publications, such as U.S. Patent Application Serial No. 08/905,286, assigned to the same assignee as the present invention, the disclosure of which is incorporated herein by reference in its entirety. U.S. Patent Application Serial No. 08/905,286 describes, *inter*

alia, the steps of programming, reading and erasing NROM cells. U.S. Patent Application Serial No. 09/730,586, also assigned to the same assignee as the present invention and incorporated herein by reference in its entirety, describes an additional method for programming and erasing an NROM array.

[0022] NROM cells operated in accordance with the present invention may be single bit cells or alternatively, they may store or represent more than one bit. In the latter case, for example, two individual bits, a left-side bit and a right-side bit, may be stored in physically different storage areas of the charge-trapping region layer associated with the cell. Moreover, each cell in accordance with the present invention may be a single level or multi-level cell. In the latter case, the storage areas within the cell may be programmed to different voltage levels.

[0023] Fig. 2A shows a plurality of bit lines $BL_{(1)}$ through $BL_{(8)}$, a plurality of word lines $WL_{(1)}$ through $WL_{(3)}$, a column decoder 20 that may include select transistors and additional peripheral devices, and a row decoder 30 that may include select transistors and additional peripheral devices. The following discussion assumes a close-to-ground read operation, such as that used for NROM cells and described in U.S. Patent No. 6,128,226, and assigned to the same assignee of the present invention. However, this invention is also applicable for other, non-close-to-ground types of reads and to arrays of other types of memory cells.

[0024] According to an exemplary embodiment of the invention, a pair of adjacent cells such as MC_3 and MC_4 may be connected to the same word line $WL_{(2)}$ and share an inside common bit line, e.g., BL_4 in this example,

which may be the reading node. The outside bit lines, BL_3 and BL_5 for the same example, may be coupled to a voltage source. The two adjacent cells MC_3 and MC_4 may hold the same data and may be read or sensed in parallel by the same sensing circuit (not shown). In accordance with this embodiment, there is substantially no NE in this configuration because the reading node has no neighbor cells. In addition, this configuration may provide approximately twice the current than the current in a single bit per cell read mode, which is described, for example, in U.S. Patent No. 5,768,192, assigned to same assignee as the present invention.

[0025] The reading node may act as the source of the cells, e.g., for source-side read, shown in Fig. 2A, or as the drain of the cells, e.g., for drain-side read, shown in Fig. 2B. In the first case, the outside bit lines, BL_3 and BL_5, may be driven to a positive low voltage, e.g., in the range of 1-2V, while in the second case the outside bit lines may be grounded or brought close to ground. Driving of the outside or non-shared bit lines may be done either directly or through switches and the inside or shared reading node may be coupled directly or through switches to a sensing circuit that may determine the state of the cells being read.

[0026] In accordance with the embodiment depicted in Figs. 2A and 2B, when the memory cells in the array are NROM cells, the cells may be used in a single bit mode. In general, NROM cells may preferably be reverse read, e.g., if programming is performed in one direction with a first bit line acting as the source, and a second bit line acting as the drain, then the read operation is performed in the reverse direction, e.g., with the second bit line acting as the source, and the first bit line acting as the drain. Thus, as shown

in Fig. 2A, the cells may preferably store data in the storage areas close to the shared common bit lines BL_4 in the source side read case, or alternatively, as shown in Fig. 2B, in the storage areas close to the outside bit lines BL_3 and BL_5 in the drain side read case, as shown in Fig. 2B.

[0027] In accordance with the embodiment of Fig. 2B, in the drain-side read case, operation of NROM cells in a forward read configuration may also be applicable, whereby program and read may be performed in the same direction. Although doing so may require more aggressive programming, such a configuration may simplify the peripheral circuitry, for example column decoder 20 and row decoder 30, in particular.

[0028] It is worth noting that an important criterion in measuring performance of a memory array is access time. One of the factors determining the access time of a memory array is the level of the readout signal that a memory cell can develop during a certain time. This signal level should desirably be large enough in order to reliably sense the contents of the cell. The signal developed by the cell during sensing is typically a function of its current. Therefore, increasing the current of the cell may decrease its readout time. As such, one of the possible benefits of some embodiments of the present invention is an increase in cell current, and therefore, a reduction of readout time.

[0029] Reference is now made to Figs. 3A and 3B which are block diagram illustrations of a group of memory cells in a VG NVM array 10 being read using possible methods for read operation in a two cell per two bits configuration in accordance with an embodiment of the invention. Components of the array of Figs. 3A and 3B that are similar to those of

Figs. 2A and 2B are designated with the same reference labels, and the description is not repeated for the sake of brevity.

[0030] According to an embodiment of the invention, a pair of adjacent cells MC_3 and MC_4 may be on the same word line $WL_{(2)}$, the common bit line, BL_4 in this example may be the "reading" node, and the outside bit lines, BL_3 and BL_5 for the same example may be coupled to the same voltage source. The two adjacent cells MC_3 and MC_4 which may be accessed simultaneously may hold the same data and may be read concurrently. This configuration may provide approximately twice the current than the current in a "single cell per bit" case, which is described, for example, in U.S. Patent No. 5,768,192, assigned to same assignee of the present invention. In addition, in accordance with this embodiment, there is substantially no NE since the "reading" node is substantially unaffected by undesired current from neighbor cells.

[0031] In accordance with the embodiment of Figs. 3A and 3B, an NROM cell may store two distinct bits of data, and may therefore, achieve twice the density, compared to the two cells per bit configuration. The operation of the NROM cells in this configuration may be a two bit per cell operation, whereby program and read may be performed in reverse directions.

[0032] Fig. 3A describes a method for source-side read operation of memory cells in a VG NVM array 10 in a two cell per two bits configuration in accordance with an embodiment of the invention. When adjacent cells MC_2 and MC_3 are source-side read, the data that may be read when accessing them may be stored on the first storage areas close to the common bit line

BL_3. These first storage areas may be read substantially simultaneously and may contain substantially the same data. In accordance with this embodiment, the second storage areas of cells MC_2 and MC_3, e.g., the storage area close to the outside bit lines, BL_2 and BL_4, respectively, may correspond to the data read when accessing cells MC_1 and MC_2 or cells MC_3 and MC_4, respectively.

[0033] Fig. 3B describes a method for drain-side read operation of memory cells in a VG NVM array 10 in a two cell per two bits configuration in accordance with an embodiment of the invention. When adjacent cells MC_2 and MC_3 are drain-side read, the data that may be read when accessing them may be stored in the second storage areas close to the outside bit lines BL_2 and BL_4. These second storage areas may be read substantially at the same time and may contain substantially the same data. In accordance with this embodiment, the first storage areas of cells MC_2 and MC_3, e.g., close to the inside shared bit line BL_3, may correspond to the data that may be read when accessing cells MC_1 and MC_2 or MC_3 and MC_4, respectively.

[0034] In the source-side read operation the outside bit lines may be driven to a positive low voltage, e.g., in the range of 1-2V, while in the drain-side read operation the outside bit lines may be driven to ground or close to ground potential. The outside bit lines may be driven either directly or through switches and the reading node may be coupled directly or through switches to a sensing circuit that may determine the state of the cells being read.

[0035] Reference is now made to Figs. 4A-4C which are block diagram illustrations of a group of memory cells in a VG NVM array 10 being read

using possible methods for read operation of memory cells in a VG NVM array in N pairs of cells per bit of data, or N pairs of cells per two bits of data in accordance with an embodiment of the invention. Components of the array of Figs. 4A-4C that are similar to that of Fig. 2A are designated with the same reference labels, and the description is not repeated for the sake of brevity.

[0036] In accordance with the embodiment depicted in Figs. 4A-4C, N pairs of adjacent cells in single bit mode or in two bit mode may be accessed and read substantially simultaneously. When the cells are operated in a single bit mode, the N pairs may store one bit of data, and when the cells are operated in two bits mode, the N pairs may store two bits of data.

[0037] The N pairs of adjacent cells may share the same word line, as shown in Fig. 4A, or the same reading bit lines and outside bit lines, as shown in Fig. 4B. Alternatively, the N pairs of adjacent cells may share a combination of word lines and bit lines, as shown in Fig. 4C.

[0038] Referring now to Fig. 4A, the N pairs of adjacent cells may share the same word line, e.g., $W_{(2)}$, the reading bit lines of all pairs, e.g., BL_2, BL_4, and BL_6 in, may be coupled, either directly or through switches, to a sensing circuit, and the adjacent bit lines of all pairs, e.g., BL_3 and BL_5 in, may be coupled together, either directly or through switches, and driven to the same voltage source.

[0039] Referring now to Fig. 4B, the N pairs of adjacent cells may share the same inside bit lines and outside bit lines, e.g., MC_3 and MC_4, and MC'_3 and MC'_4 may share BL_3 and BL_5, and the same word lines, e.g., $WL_{(2)}$ and $WL_{(1)}$. Accordingly, the bit lines and word lines connected to the pairs of

cells may be driven substantially at the same time when accessing the pairs for read operation.

[0040] Referring now to Fig. 4C, a third configuration of this embodiment of the invention, the N pairs of adjacent cells may share a combination of word lines and bit lines. For the example of N=4, shown in Fig. 4C, a number, K, of the N pairs of cells, e.g., the two pairs of cells MC_3 to MC_6, may share the same word line, e.g., $WL_{(2)}$. N-K pairs of cells, e.g., two pairs of cells MC'_3 to MC'_6 may be placed on one or more word lines, e.g., $WL_{(1)}$ in Fig. 4C, and may share the same bit lines as the first K pairs. The reading bit lines, e.g., BL_3, BL_5, and BL_7 of the cells may be coupled together, either directly or through switches, to a sensing circuit. The adjacent bit lines of the cells divided to pairs, e.g., BL_4 and BL_6, and their word lines, $WL_{(2)}$ and $WL_{(1)}$, may be coupled together, either directly or through switches, and may be driven to the same voltage source.

[0041] In accordance with any of the described embodiments an increased amount of current may be sensed and the neighbor effect may be reduced or eliminated. Thus, a fast and reliable read operation may be achieved.

[0042] In an exemplary embodiment of the present invention, adjacent cells that are read together may be programmed and/or erased to be in the same state. It will be understood that the present invention may be practiced with any suitable method of programming and erasing cells. Thus, in accordance with an embodiment of the present invention the VG NVM array may be programmed by, for example, applying a series of programming pulses to either the drain or the gate of the pertinent memory cells in the

array. For example, a programming pulse applied to the drain may initiate at an amplitude of 4.5V. A programming pulse applied to the gate may, for example, initiate at 8.0V.

[0043] In accordance with an embodiment of the present invention, a VG NVM array may be programmed by applying programming pulses to pairs of cells or combinations of pairs of cells in the VG NVM array simultaneously or in serial order. Thus, for example, in an embodiment of the present invention utilizing simultaneous programming of, for example, N pairs of cells, all 2N cells may be programmed simultaneously by identical programming pulses. Alternately, each of the N pairs of cells may be programmed individually. In another embodiment of the invention, a combination of the simultaneous and serial programming methods may be utilized. Thus, in such an embodiment, some of the N pairs of cells may be programmed simultaneously until all N pairs are programmed.

[0044] Reference is now made to Fig. 5 which is a block diagram illustration of a VG NVM array, operable in accordance with embodiments of the present invention. The global bit lines (GBL) of the VG NVM array, e.g., $GBL_{(N)}$ and $GBL_{(N+1)}$, may be connected to local bit lines (LBL), e.g., BL_0 through BL_7, through select devices, SEL_1 through SEL_7. In accordance with this embodiment the local bit lines may serve as the local "reading" bit lines or as the bit lines that may be coupled to the same voltage source. The LBL's may be connected through the GBLs to peripheral circuits, sense amplifiers, or voltage drivers.

[0045] In accordance with an embodiment of the present invention, a portion of the LBLs that may be coupled to the same voltage source, e.g., the

non-"reading" LBL's, may be coupled together without select devices. Thus, the size of the array may be reduced due to the reduced number of select devices. Reference is now made to Fig. 6 which is a block diagram illustration of a VG NVM array, operable in accordance with this embodiment of the present invention. In this configuration, the global bit lines (GBL) of the VG NVM array, e.g., $GBL_{(M)}$ and $GBL_{(M+1)}$, may be connected to the local bit lines that serve as the local "reading" bit lines, e.g., BRL_2, BRL_4, BRL_6, BRL_8 etc. In accordance with this embodiment the non-"reading" local bit lines, e.g., $BNRL_1$, $BNRL_3$, $BNRL_5$, $BNRL_7$ etc., may be coupled together to the same voltage source, for example, through WL_1.

[0046] It will be appreciated by persons skilled in the art that the present invention is not limited by what has been particularly shown and described herein above. For example, although particular array structure has been described in the particular method above, it will be understood that other array structures and configurations may be employed within the bounds of the invention, and that the invention is not limited in this regard. For example, floating gate transistors may be used instead of NROM cells, and the example in Fig. 4C may also be changed.